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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,199	02/22/2002	Kathleen Ann Gehoski	CR01-031	2871

23330 7590 05/13/2003

MOTOROLA, INC.
CORPORATE LAW DEPARTMENT - #56-238
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EXAMINER	
GOUDREAU, GEORGE A	

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 05/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

HG

Office Action Summary

Application No.	Applicant(s)
10-081,199	Gehoski et al
Examiner	**Group Art Unit**
George Goldrean	1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 (MONTH(S)) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 2-02-01 (Re: paper #1)

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-22 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-22 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____ .

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____ .

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

16. Claims 1-3, 5, 7-8, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lothian et. al. (5,981,319).

Lothian et. al. disclose a process for forming a transistor on the surface of a wafer by forming a metallic T gate between source/ drain regions on the surface of the wafer. The T gate is formed on the surface of the wafer using the following process steps:

-A patterned, first photo resist layer (44) is formed onto the surface of the wafer (43).;

-The surface of the first photo resist layer is hardened (i.e.-polymerized) by exposing it to a plasma at a temperature of (50-100) C. The plasma is comprised of ions of any of N, O, Ar, Xe, or He.;

-A patterned, second photo resist layer (48) is formed onto the surface of the first photo resist layer.;

-Metallic conductive layers are deposited onto the surface of the second photo resist layer as well as inside the T gate shaped opening formed in the photo resist layers.; and

-The photo resist layers, and the excess metallic conductive layers are removed from the surface of the wafer using a lift off process in which the substrate is immersed in a solvent. (Thus, a T gate is left behind on the surface of the wafer to form a transistor.) This is discussed specifically in columns 3-4; and discussed in general in columns 1-6. This is shown in figures 1-13.

17. Claims 1-3, 5, 7-9, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Furukawa et. al. (6,387,783).

Furukawa et. al. disclose a process for forming a transistor on the surface of a wafer by forming a metallic T gate between source/ drain regions on the surface of the wafer. The T gate is formed on the surface of the wafer using the following process steps:

-A patterned, first hybrid photo resist layer (201) is formed onto the surface of the wafer.;

-The first patterned photo resist layer is hardened (i.e.-polymerized) by baking it, and exposing it to UV light.;

-A patterned, second photo resist layer (207) is formed onto the surface of the first photo resist layer.;

-Metallic conductive layers are deposited onto the surface of the second photo resist layer, and inside the T gate shaped opening formed inside the patterned photo resist layers.;

-The excess metallic conductive layers as well as the second photo resist layer is removed from the surface of the wafer using a lift off process in which the substrate is immersed in a solvent.;

-The first photo resist layer is removed from the surface of the wafer using a plasma etchant which is comprised of either O3 or O2. (Thus, a T gate is left behind on the surface of the wafer to form a transistor.)

This is discussed specifically in columns 3-5; and discussed in general in columns 1-10. This is shown in figures 1-3.

18. Claims 1-3, 5, 7-9, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kang et. al. (JP 07-201,889).

Kang et. al. disclose a process for forming a transistor on the surface of a wafer by forming a metallic T gate between source/ drain regions on the surface of the wafer. The T gate is formed on the surface of the wafer using the following process steps:

-A patterned, first photo resist layer (20) is formed onto the surface of the wafer (10).;

-The surface of the first photo resist layer is hardened (i.e.-polymerized) by exposing it to a heat source at a temperature of greater than 150 C.;

-A patterned, second photo resist layer (40) is formed onto the surface of the first photo resist layer.;

-Metallic conductive layers (50) are deposited onto the surface of the second photo resist layer as well as inside the openings formed in the photo resist layers.

-The excess metallic conductive layers, and the second photo resist layer are removed from the surface of the wafer using a lift off process in which the substrate is immersed in a solvent.; and

-The first photo resist layer is removed from the surface of the wafer using a plasma etchant which is comprised of O2. (Thus, a T gate is left behind on the surface of the wafer to form a transistor.)

This is discussed specifically in the abstract; and discussed in general in columns 1-8. This is shown in figures 1-6.

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

21. Claims 4, 9-13, 15-17, 19-20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lothian et. al. as applied in paragraph 16 above.

Lothian et. al. as applied in paragraph 16 above fail to specifically disclose the following aspects of applicant's claimed invention:

-the specific usage of the types of resist materials which are claimed by the applicant to form the different resist layers; and

-the specific means which are claimed by the applicant for removing the photo resist layers using a two step process

It would have been obvious to one skilled in the art to form any of the photo resist layers in the process taught above out of any of the specific types of materials which are claimed by the applicant based upon the following. The usage of the specific types of materials which are claimed by the applicant is conventional or at least well known in the semiconductor fabrication arts. (The examiner takes official notice in this regard.) Further, this simply involves the usage of an alternative, and at least equivalent means for providing photo resist layers on a wafer to the specific means which are taught above.

It would have been obvious to one skilled in the art to use the specific type of two step process which is claimed by the applicant for removing the photo resist layers from the wafer in the process taught above. The specific two step means for removing the photo resist layers from the wafer in the process taught above which is claimed by the applicant is conventional or at least well known in the semiconductor fabrication arts. (The examiner takes official notice in this

regard.) Further, this simply involves the usage of an alternative, and at least equivalent means for removing the photo resist layers on the wafer in the process taught above to the specific means which are taught above.

22. Claims 4, 6, 10-17, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et. al. (6,387,783) as applied in paragraph 17 above.

Furukawa et. al. as applied in paragraph 17 above fail to specifically disclose the following aspects of applicant's claimed invention:

-the specific usage of the types of resist materials which are claimed by the applicant to form the different resist layers; and

-the specific usage of DUV light to harden (i.e.-polymerize) the first photo resist layer in the process taught above

It would have been obvious to one skilled in the art to form any of the photo resist layers in the process taught above out of any of the specific types of materials which are claimed by the applicant based upon the following. The usage of the specific types of materials which are claimed by the applicant is conventional or at least well known in the semiconductor fabrication arts. (The examiner takes official notice in this regard.) Further, this simply involves the usage of an alternative, and at least equivalent means for providing photo resist layers on a wafer to the specific means which are taught above.

It would have been obvious to one skilled in the art to specifically employ DUV type UV radiation to hardened (i.e.-polymerize) the first photo resist layer in the process taught above

based upon the following. The reference generically teaches the usage of any type of UV light to harden (i.e.-polymerize) the first photo resist layer. The specific usage of DUV light simply represents the usage of a specific subset of UV radiation.

23. Claims 4, 10-13, 15-17, 19-20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang et. al. as applied in paragraph 18 above.

Kang et. al. as applied in paragraph 18 above fail to specifically disclose the following aspects of applicant's claimed invention:

-the specific usage of the types of resist materials which are claimed by the applicant to form the different resist layers

It would have been obvious to one skilled in the art to form any of the photo resist layers in the process taught above out of any of the specific types of materials which are claimed by the applicant based upon the following. The usage of the specific types of materials which are claimed by the applicant is conventional or at least well known in the semiconductor fabrication arts. (The examiner takes official notice in this regard.) Further, this simply involves the usage of an alternative, and at least equivalent means for providing photo resist layers on a wafer to the specific means which are taught above.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag

Primary Examiner

AU 1763